National Semiconductor

# ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
# 8-Bit μP Compatible A/D Converters

## General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

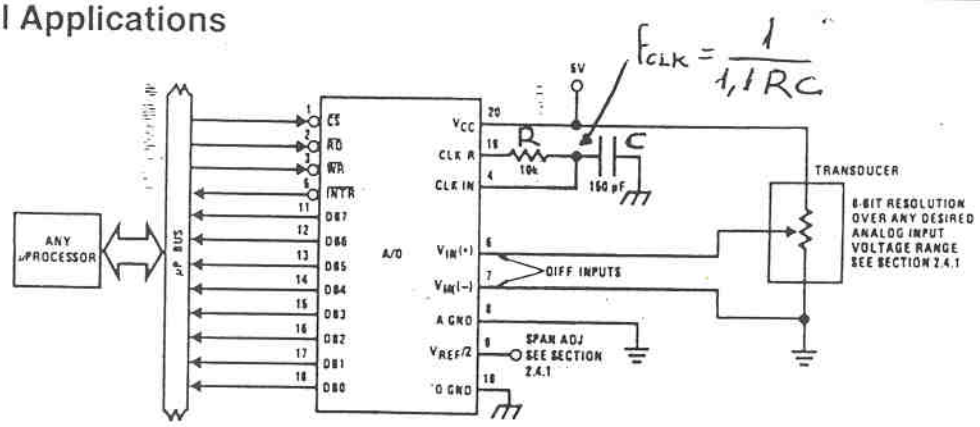
## Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 $V_{DC}$, 2.5 $V_{DC}$, or analog span adjusted voltage reference

## Key Specifications

- Resolution: 8 bits
- Total error: ± ¼ LSB, ± ½ LSB and ± 1 LSB
- Conversion time: 100 μs

## Typical Applications

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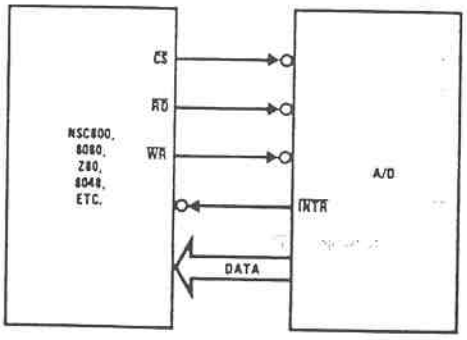
8080 Interface

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| Part Number | Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity) | | |
|---|---|---|---|
| | Full-Scale Adjusted | $V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments) | $V_{REF}/2$ = No Connection (No Adjustments) |
| ADC0801 | ± ¼ LSB | | |
| ADC0802 | | ± ½ LSB | |
| ADC0803 | ± ½ LSB | | |
| ADC0804 | | ± 1 LSB | |
| ADC0805 | | | ± 1 LSB |

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 3) | 6.5V |
| Voltage | |
| Logic Control Inputs | −0.3V to +18V |
| At Other Input and Outputs | −0.3V to ($V_{CC}$ + 0.3V) |
| Lead Temp. (Soldering, 10 seconds) | |
| Dual-In-Line Package (plastic) | 260°C |
| Dual-In-Line Package (ceramic) | 300°C |
| Surface Mount Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |
| Storage Temperature Range | −65°C to +150°C |
| Package Dissipation at $T_A$ = 25°C | 875 mW |
| ESD Susceptibility (Note 10) | 800V |

## Operating Ratings (Notes 1 & 2)

| | |
|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| ADC0801/02LJ | $-55°C \le T_A \le +125°C$ |
| ADC0801/02/03/04LCJ | $-40°C \le T_A \le +85°C$ |
| ADC0801/02/03/05LCN | $-40°C \le T_A \le +85°C$ |
| ADC0804LCN | $0°C \le T_A \le +70°C$ |
| ADC0802/03/04LCV | $0°C \le T_A \le +70°C$ |
| ADC0802/03/04LCWM | $0°C \le T_A \le +70°C$ |
| Range of $V_{CC}$ | 4.5 $V_{DC}$ to 6.3 $V_{DC}$ |

## Electrical Characteristics

The following specifications apply for $V_{CC}$ = 5 $V_{DC}$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK}$ = 640 kHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ADC0801: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) | | | ± ¼ | LSB |
| ADC0802: Total Unadjusted Error (Note 8) | $V_{REF}/2$ = 2.500 $V_{DC}$ | | | ± ½ | LSB |
| ADC0803: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) | | | ± ½ | LSB |
| ADC0804: Total Unadjusted Error (Note 8) | $V_{REF}/2$ = 2.500 $V_{DC}$ | | | ± 1 | LSB |
| ADC0805: Total Unadjusted Error (Note 8) | $V_{REF}/2$-No Connection | | | ± 1 | LSB |
| $V_{REF}/2$ Input Resistance (Pin 9) | ADC0801/02/03/05<br>ADC0804 (Note 9) | 2.5<br>0.75 | 8.0<br>1.1 | | kΩ<br>kΩ |
| Analog Input Voltage Range | (Note 4) V(+) or V(−) | Gnd−0.05 | | $V_{CC}$ + 0.05 | $V_{DC}$ |
| DC Common-Mode Error | Over Analog Input Voltage Range | | ± 1/16 | ± ⅛ | LSB |
| Power Supply Sensitivity | $V_{CC}$ = 5 $V_{DC}$ ± 10% Over Allowed $V_{IN}$(+) and $V_{IN}$(−) Voltage Range (Note 4) | | ± 1/16 | ± ⅛ | LSB |

## AC Electrical Characteristics

The following specifications apply for $V_{CC}$ = 5 $V_{DC}$ and $T_A$ = 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_C$ | Conversion Time | $f_{CLK}$ = 640 kHz (Note 6) | 103 | | 114 | μs |
| $T_C$ | Conversion Time | (Note 5, 6) | 66 | | 73 | $1/f_{CLK}$ |
| $f_{CLK}$ | Clock Frequency<br>Clock Duty Cycle | $V_{CC}$ = 5V, (Note 5)<br>(Note 5) | 100<br>40 | 640 | 1460<br>60 | kHz<br>% |
| CR | Conversion Rate in Free-Running Mode | $\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 $V_{DC}$, $f_{CLK}$ = 640 kHz | 8770 | | 9708 | conv/s |
| $t_{W(\overline{WR})L}$ | Width of $\overline{WR}$ Input (Start Pulse Width) | $\overline{CS}$ = 0 $V_{DC}$ (Note 7) | 100 | | | ns |
| $t_{ACC}$ | Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) | $C_L$ = 100 pF | | 135 | 200 | ns |
| $t_{1H}$, $t_{0H}$ | TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) | $C_L$ = 10 pF, $R_L$ = 10k (See TRI-STATE Test Circuits) | | 125 | 200 | ns |
| $t_{WI}$, $t_{RI}$ | Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$ | | | 300 | 450 | ns |
| $C_{IN}$ | Input Capacitance of Logic Control Inputs | | | 5 | 7.5 | pF |
| $C_{OUT}$ | TRI-STATE Output Capacitance (Data Buffers) | | | 5 | 7.5 | pF |
| **CONTROL INPUTS** [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] | | | | | | |
| $V_{IN}$ (1) | Logical "1" Input Voltage (Except Pin 4 CLK IN) | $V_{CC}$ = 5.25 $V_{DC}$ | 2.0 | | 15 | $V_{DC}$ |

$f_{CLK} = \frac{1}{1,1\,R \cdot C}$

## AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CONTROL INPUTS** [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] | | | | | | |
| $V_{IN}$ (0) | Logical "0" Input Voltage (Except Pin 4 CLK IN) | $V_{CC} = 4.75\ V_{DC}$ | | | 0.8 | $V_{DC}$ |
| $I_{IN}$ (1) | Logical "1" Input Current (All Inputs) | $V_{IN} = 5\ V_{DC}$ | | 0.005 | 1 | $\mu A_{DC}$ |
| $I_{IN}$ (0) | Logical "0" Input Current (All Inputs) | $V_{IN} = 0\ V_{DC}$ | −1 | −0.005 | | $\mu A_{DC}$ |
| **CLOCK IN AND CLOCK R** | | | | | | |
| $V_T+$ | CLK IN (Pin 4) Positive Going Threshold Voltage | | 2.7 | 3.1 | 3.5 | $V_{DC}$ |
| $V_T-$ | CLK IN (Pin 4) Negative Going Threshold Voltage | | 1.5 | 1.8 | 2.1 | $V_{DC}$ |
| $V_H$ | CLK IN (Pin 4) Hysteresis $(V_T+) - (V_T-)$ | | 0.6 | 1.3 | 2.0 | $V_{DC}$ |
| $V_{OUT}$ (0) | Logical "0" CLK R Output Voltage | $I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$ | | | 0.4 | $V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" CLK R Output Voltage | $I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$ | 2.4 | | | $V_{DC}$ |
| **DATA OUTPUTS AND $\overline{INTR}$** | | | | | | |
| $V_{OUT}$ (0) | Logical "0" Output Voltage Data Outputs<br>$\overline{INTR}$ Output | $I_{OUT} = 1.6\ mA$, $V_{CC} = 4.75\ V_{DC}$<br>$I_{OUT} = 1.0\ mA$, $V_{CC} = 4.75\ V_{DC}$ | | | 0.4<br>0.4 | $V_{DC}$<br>$V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" Output Voltage | $I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$ | 2.4 | | | $V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" Output Voltage | $I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$ | 4.5 | | | $V_{DC}$ |
| $I_{OUT}$ | TRI-STATE Disabled Output Leakage (All Data Buffers) | $V_{OUT} = 0\ V_{DC}$<br>$V_{OUT} = 5\ V_{DC}$ | −3 | | 3 | $\mu A_{DC}$<br>$\mu A_{DC}$ |
| $I_{SOURCE}$ | | $V_{OUT}$ Short to Gnd, $T_A = 25°C$ | 4.5 | 6 | | $mA_{DC}$ |
| $I_{SINK}$ | | $V_{OUT}$ Short to $V_{CC}$, $T_A = 25°C$ | 9.0 | 16 | | $mA_{DC}$ |
| **POWER SUPPLY** | | | | | | |
| $I_{CC}$ | Supply Current (Includes Ladder Current)<br><br>ADC0801/02/03/04LCJ/05<br>ADC0804LCN/LCV/LCWM | $f_{CLK} = 640\ kHz$, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$ | | 1.1<br>1.9 | 1.8<br>2.5 | mA<br>mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

**Note 3:** A zener diode exists, internally, from $V_{CC}$ to Gnd and has a typical breakdown voltage of 7 $V_{DC}$.

**Note 4:** For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the $V_{CC}$ supply. Be careful, during testing at low $V_{CC}$ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog $V_{IN}$ does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 $V_{DC}$ to 5 $V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.950 $V_{DC}$ over temperature variations, initial tolerance and loading.

**Note 5:** Accuracy is guaranteed at $f_{CLK} = 640\ kHz$. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

**Note 6:** With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

**Note 7:** The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

**Note 8:** None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

**Note 9:** The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from $V_{CC}$ to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

**Note 10:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.